D. Remarks

Rejection of Claims 1-3, 7, 8, 10, 12, 13 and 15 Under 35 U.S.C. §103(a), based on Applicants' Background Art (*Background Art*) in view of U.S. Patent No. 5,515,226 (*Tailliet*).

The semiconductor integrated circuit device of claim 1 includes a plurality of IGFETs coupled to a corresponding I/O terminal through a corresponding first resistance. A first clamping circuit is coupled to each I/O terminal. A second clamping circuit corresponds to each IGFET. Each second clamping circuit includes a second clamping device and the corresponding first resistance. Each second clamping device has a first terminal connected to a gate electrode of the corresponding IGFET and a second terminal connected to a source/drain terminal of the corresponding IGFET and a supply potential wiring. Each first clamping device is coupled to one second clamping device through a second resistance. At least two of the second clamping circuits vary from one another.

No Motivation for Proposed Combination – Rejection's Rebuttal Argument Improper

As is well established, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found in either the references themselves or in the knowledge generally available to one of ordinary skill in the art.

In Applicants' previous response to Office Action, grounds for traversing this rejection were set forth based on a lack of motivation to combine the references. In Applicants' argument, it was shown that the *Background Art* is directed to a charge device mode CDM model, while *Tailliet* was directed to HBM or MM models. Evidence in support of the argument was presented by citations to the references relied upon by the rejection.

To rebut Applicants' showing, the rejection relies on the following rebuttal argument:

> Regarding claims 1-3, 5-7, 10, 11, 13-15 applicant argued that the Tailliet reference is not related to a CDM mode, but his argument is not shown in claim 1.[1]

[1] See the Final Office Action, dated 8/22/03, Page 6, Lines

This is an improper standard for obviousness, and thus cannot rebut Applicants' showing.

Motivation for combining references must come from the references themselves. Applicants are not arguing that the proposed combination does not show any particular claim limitation. Applicants are arguing that there is no motivation for combining the references, based on the teachings of the references themselves. What is or is not included in Applicants' claims is irrelevant to such an argument. Thus, the rejections rebuttal argument, relying on Applicants' claim limitations cannot rebut Applicants' clear showing that motivation for combining the *Background Art* with *Tailliet* is lacking.

Because the above rebuttal argument is based on an improper standard, Applicants respectfully request that this ground for rejection be withdrawn.

Applicants' resubmit the evidence that is believed to establishing that there is no motivation/suggestion for combining the *Background Art* with *Tailliet.*

Differences between the CDM mode and HBM and MM models are set forth in Applicants' Specification:

> For appraisal according to HBM and MM models, electric charges can be applied between two predetermined terminals of a device. In contrast, for appraisal according to a CDM model, a package and a chip of the device can be charged with electricity. Such charge can then be discharged to an outside location through terminals of the device.[2]

Tailliet is not related to a CDM model, and teaches away from such an arrangement by showing an MM or HBM type model. This is clearly shown by all teachings set forth in *Tailliet*:

The "Background and Summary of Invention" of *Tailliet* only describes an HBM or MM type model:

> FIG. 2 shows the simplest configuration generally used to protect a pad Pj connected by a conductor Cj to an input Ej... The input Ej... must be protected against electrostatic discharges.[3]

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[2] Applicants' Specification, Page 2, Lines 5-10, emphasis added.
[3] *Tailliet*, Col. 2, Lines 9-14.

> The electrostatic discharges... are diverted towards the ground bus BM, thus preventing overvoltages from appearing at the conductor Cj and hence at the input Ej. The arrangement is the same for the other pads...[4]

Thus, the "Background and Summary of Invention" of *Tailliet* teaches the application of charge between two predetermined terminals of a device (Pad Pj and Pad P1), which is the HBM or MM mode, and not the CDM model.

The remainder of *Tailliet* is no different, and once more shows only an HBM or MM mode, and provides no teachings related to the CDM model:

> Indeed, the electrostatic discharge on the pad Pj causes the limiter EC1j to be placed in a state of conduction, shunting the discharge current towards the ground BM and from there towards the ground pad P1...[5]

> The protection device according to the invention works as follows: when an electrostatic discharge reaches the access pad Pj, the first limiter EC1j becomes conductive... If the discharge current is equal to some amperes, a voltage drop of several volts (for example about 20 volts for a current of 4 amperes) may occur in the ground bus BM between the pad P1 and the pad Pj.[6]

Thus, the remainder of *Tailliet* teaches the application of charge between two predetermined terminals of a device (Pad Pj and Pad P1). Once again, this is the HBM or MM mode, and not the CDM model.

Applicants' believe that the above showing clearly establishes that the requisite motivation/suggestion for a prima facie case of obviousness has not been established. In addition, the rejection's rebuttal argument is improper. Accordingly, this ground for rejection is traversed.

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[4] *Tailliet*, Col. 2, Lines 24-28.
[5] *Tailliet*, Col. 3, Lines 54-57.

All Limitations Not Shown or Suggested by Proposed Combination of the Rejection – Rebuttal Argument

The combination of references does not show all limitations of claim 1. As noted above, claim 1 recites second clamping circuits, each corresponding to a different IGFET, where at least two such clamping circuits vary from one another.

As noted previously, the rejection admits that the *Background Art* fails to show such a limitation.[7] Further, Applicants have previously addressed numerous rejection rationales showing that such a limitation is not shown or suggested by *Tailliet*, either.

To rebut Applicants showing the rejection argues the following:

> [A]pplicant also argued that the Tailliet reference does not show variation [between] two second limiters, however, Tailliet teaches a plurality of second voltage limiters vary from each other by the internal resistor (Rj) (see col. 4, lines 34-47). Thus applicant's arguments of claim 1 do not overcome the Tailliet reference.[8]

Applicants have previously addressed this reasoning. In particular, Applicants have shown that the above contention, that reference shows multiple internal resistors (Rj) that vary from one another, is not supported by the reference.

The portion of *Tailliet* relied upon by the rejection does not show variation between second limiters. The cited portion is set forth below, in full.

> However, if the input Ej is a field-effect transistor gate or another element with high input impedance, the value of the resistor Rj is not of critical importance. It will be chosen so as to be sufficiently high to limit the current in the second limiter EC2j to an acceptable value (that depends on the dimensions of the limiter EC2j).

The above is directed to the selection of a resistor value Rj, and provides no suggestion for

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[6] *Tailliet*, Col. 3, Lines 48-60.

[7] See the Final Office Action, dated 8/22/03, Page 2, third and fourth lines from the bottom.

providing two different values for Rj.

In summary, Applicant believes a fair reading of the above shows that the excerpt relied upon by the rejection describes how one resistor value is selected, and does not show or suggest the selection of different values for different resistors.

For all of these reasons, a prima facie case of obviousness has not been established for claim 1, and this ground of rejection is traversed.

Various claims depending from claim 1 are believed to include additional limitations not shown by the cited combination.

Claim 3 recites that at least two second clamping devices vary by having second clamping circuits with different capabilities. Claim 15 recites second clamping devices with different construction.

As noted above with regard to claim 1, *Tailliet* provides no description of how one voltage limiter may or may not differ from another, let alone how such limiters can differ in capability. Thus, a prima facie case of obviousness has not been established for these claims, either.

Claim 8 recites that a majority of at least one first resistance includes non-wiring structures. Applicant previously noted that this limitation was not addressed by the rejection. In response, the final rejection refers to the first Office Action issued in the present case:

> Regarding to claim 8, applicant argued that the limitations of claim 8 are not addressed. However, these limitations are addressed in the rejections sent on 10/07/2002. Therefore, applicant's arguments of claim 8 are not persuasive.[9]

However, Applicants have previously shown that the argument set forth for claim 8 in the Office Action of 10/07/02 were in error. Applicants' response is set forth below.

> Claim 8 recites that a majority of at least one first resistance includes non-wiring structures. Claim 9 indicates that a first resistance includes an effective channel resistance of an

[8] See the Final Office Action, dated 8/22/03, Page 6, Lines 17-21.

input path IGFET. The rejection of claims 8 and 9 relies on the following rationale.

> [The *Background Art*] discloses that the first resistance R114 includes an effective channel resistance of an input path transistor (end to end path through the transistor 112a).[10]

> Applicants' *Background Art* indicates that an input resistor (e.g., 114) is illustrative of an input resistance and an input wiring resistance inherent in a semiconductor device. Nothing in Applicants' *Background Art* indicates that a transistor that is being protected (i.e., 112) is included in an input resistance. Clarification for the basis of this rejection is respectfully requested.[11]

Thus, the previous ground of rejection, relied upon in the final rejection, argues that a "first resistance" is shown by transistor 114. However, as emphasized by Applicant's response, transistor 112a has nothing to do with an input resistance, thus cannot show the limitations of claim 8.

Claim 12 adds that a second terminal of each second clamping device is connected to a second supply terminal different from a first supply terminal. Thus, Applicant's claim 12 recites two different supply terminals (first and second). To show the limitations of claim 12, the final rejection relies on the following reasoning:

> Tailliet discloses the first clamping circuit (EC1j) and second clamping circuit (EC2j) are connected to different power supply terminals (between Pj and P1, see fig. 3).[12]

> Regarding claim 12, applicant argued that P1 is not a power supply terminal. Tailliet discloses P1 is a power supply terminal (col. 1, lines 52-53). Therefore, applicant's argument of claim 12 are not persuasive. [13]

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[9] See the Final Office Action, dated 8/22/03, page 7, Lines 4-6.
[10] See the Final Office Action, dated 8/22/03, Page 4, Lines 5-7.
[11] Applicant's Response to Office Action, dated 1/3/03, Page 6, Lines 15-27.
[12] See the Office Action, dated 3/17/03, Page 5, Lines 15-16.
[13] See the Office Action, dated 3/17/03, Page 7, Lines 1-3.

The latter argument of the rejection is correct. Terminal P1 is described as a power supply terminal. However, Applicants note that two different power supply terminals are not shown. The rejection argues that both Pj and P1 are supply terminals. However, Pj is not a power supply terminal, but an access pad, which sends or receives signals, not a power supply.[14]

Also, if Pj is a power supply terminal, then *Tailliet* does not show an I/O terminal, and thus cannot show numerous limitations of independent claim 1.

Thus, because the combination does not show or suggest all limitations of claim 12, a prima facie case of obviousness has not been established for this claim.

For all of the above reasons, Applicants respectfully request that the above grounds for rejection be reconsidered. The present claims 1-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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Darryl G. Walker
Attorney
Reg. No. 43,232

Darryl G. Walker
Attorney/Agent
300 South First Street
Suite 235
San Jose, CA 95113
Tel. 1-408-289-5314

[14] See *Tailliet*, Col. 1, Lines 41-46.